

a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed; and

an input/output terminal formed on the semiconductor substrate, wherein a transistor connected directly to the input/output terminal, absent any intervening elements, is one of the transistors other than a transistor having the thinnest gate insulation film.

22. (New) A semiconductor integrated circuit device according to claim 21, further comprising a power supply terminal to which an external power supply voltage is applied, wherein a transistor connected directly to the power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

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23. (New) A semiconductor integrated circuit device according to claim 21, further comprising a power supply terminal to which an external power supply voltage is applied and a ground terminal, wherein a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

24. (New) A semiconductor integrated circuit device according to claim 21, further comprising an interface circuit connected to the input/output terminal, wherein a transistor included in the interface circuit and connected directly to the input/output terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

25. (New) A semiconductor integrated circuit device according to claim 24, wherein a transistor included in the interface circuit and connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

26. (New) A semiconductor integrated circuit device according to claim 25, wherein a transistor included in the interface circuit and having a current path connected between the power supply terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

27. (New) A semiconductor integrated circuit device according to claim 24, wherein said interface circuit includes an input buffer circuit.

28. (New) A semiconductor integrated circuit device according to claim 24, wherein said interface circuit includes an output buffer circuit.

29. (New) A semiconductor integrated circuit device according to claim 24, wherein said interface circuit includes a level shifter and an output buffer circuit.

30. (New) A semiconductor integrated circuit device according to claim 29, further comprising a regulator circuit, said level shifter converting a lowered potential level signal obtained from the regulator circuit into a power supply voltage level signal to be supplied to an external terminal.

31. (New) A semiconductor integrated circuit device according to claim 30, wherein a transistor included in the level shifter and a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film.

32. (New) A semiconductor integrated circuit device comprising:  
a semiconductor substrate on which a plurality of transistors including gate insulation films of different thicknesses are formed; and

an input/output terminal formed on the semiconductor substrate, wherein a transistor always connected directly to the input/output terminal is one of the transistors other than a transistor having the thinnest gate insulation film.

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33. (New) A semiconductor integrated circuit device according to claim 32, further comprising a power supply terminal to which an external power supply voltage is applied, wherein a transistor connected directly to the power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

34. (New) A semiconductor integrated circuit device according to claim 32, further comprising a power supply terminal to which an external power supply voltage is applied and a ground terminal, wherein a transistor having a current path connected between the power supply terminal and the ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

35. (New) A semiconductor integrated circuit device according to claim 32, further comprising an interface circuit connected to the input/output terminal, wherein a transistor included in the interface circuit and connected directly to the input/output terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

36. (New) A semiconductor integrated circuit device according to claim 35, wherein a transistor included in the interface circuit and connected directly to a power supply terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

37. (New) A semiconductor integrated circuit device according to claim 36, wherein a transistor included in the interface circuit and having a current path connected between the power

supply terminal and a ground terminal is one of the transistors other than the transistor having the thinnest gate insulation film.

38. (New) A semiconductor integrated circuit device according to claim 35, wherein said interface circuit includes an input buffer circuit.

39. (New) A semiconductor integrated circuit device according to claim 35, wherein said interface circuit includes an output buffer circuit.

40. (New) A semiconductor integrated circuit device according to claim 35, wherein said interface circuit includes a level shifter and an output buffer circuit.

41. (New) A semiconductor integrated circuit device according to claim 40, further comprising a regulator circuit, said level shifter converting a lowered potential level signal obtained from the regulator circuit into a power supply voltage level signal to be supplied to an external terminal.

42. (New) A semiconductor integrated circuit device according to claim 41, wherein a transistor included in the level shifter and a device directly receiving the lowered potential level signal is the transistor having the thinnest gate insulation film.--

**REMARKS**

Favorable consideration and allowance of the instant application are requested. The final office action of June 28, 1999 in the parent of the instant application has been carefully reviewed and these remarks are responsive thereto. Claims 1-20 remain pending. Claims 10-12 and 15-20